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Patent Application

Inventor(s): Bo Soon Chang

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Application No.: 10/085,757

Title: AN INTEGRATED BACK-END INTEGRATED CIRCUIT MANUFACTURING ASSEMBLY

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						
	B						
	C						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	D							
	E							
	F							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
RJ	G	T. Olson, "Emerging Package-less Strip Designs Demand Innovative Manufacturing Approaches", Semiconductor Magazine, Vol 1, Isuue 4, April 2000, P58, 2 Sheets
RJ	H	L. Estacio, "Cypress Semiconductor Leads the Way with Advance Strip Level Tracking", Semiconductor Magazine, Vol 1, Issue 4, April 2000, P60, 1 Sheet
RJ	I	J. Pedro, L. Estacio, " Using Electronic Strip Mapping for Tracking Defects in a Fully Integrated Assembly and Test Line", 8 Sheets
RJ	J	C.T. Choon, K.R. Vadivazhagu, N.H. Sieng, :Automation / Integration Program in TAP Reality Vs Vision", Test Assembly & Packaging 1999, 8 Sheets

Examiner RJ | Date Considered 5/10/05

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.